

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Before the Board of Patent Appeals and Interferences

In re the Application

Inventor : Sethuraman, R.
Application No. : 10/530,495
Filed : April 6, 2005
For : Data Processing Apparatus Address Range
Dependent Parallelization of Instructions

APPELLANT'S REPLY
TO
EXAMINER'S ANSWER

On Appeal from Group Art Unit 2183

Date: January 5, 2010

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TABLE OF CONTENTS

	<u>Page</u>
I. REAL PARTY IN INTEREST.....	3
II. RELATED APPEALS AND INTERFERENCES.....	3
III. STATUS OF CLAIMS.....	3
IV. STATUS OF AMENDMENTS.....	3
V. SUMMARY OF CLAIMED SUBJECT MATTER.....	3
VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL.....	3
VII. ARGUMENT.....	4
VIII. CONCLUSION	9
IX. CLAIMS APPENDIX.....	10
X. EVIDENCE APPENDIX.....	10
XI. RELATED PROCEEDINGS APPENDIX.....	10

I. REAL PARTY IN INTEREST

Appellant agrees with the Examiner's statement in the Examiner's Answer.

II. RELATED APPEALS AND INTERFERENCES

See Appellant's statement in the Appellant's Appeal Brief.

III. STATUS OF CLAIMS

Appellant agrees with the Examiner's statement in the Examiner's Answer.

IV. STATUS OF AMENDMENTS

Appellant agrees with the Examiner's statement in the Examiner's Answer.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Appellant agrees with the Examiner's statement in the Examiner's Answer.

VI. GROUNDS FOR REJECTION TO BE REVIEWED ON APPEAL

Appellant agrees with the Examiner's statement in the Examiner's Answer.

VII. ARGUMENT

I. Rejection of Claims 1-5, 7 and 15-17 Under 35 USC §103 in view of Fisher and Jensen

The rejection of claims 1-5, 7 and 15-17 is in error because the references, when combined, fail to show an element cited in the independent claims.

Appellant re-asserts, as if in full, herein, the argument presented in Appellant's Appeal Brief.

In reply to the Examiner's arguments presented in the Examiner's Answer, the Examiner asserts that

"[s]ince there is no explicit memory range recited, there are a number of ways that Fisher inherently reads upon the claimed limitation. If the memory range is inclusive of the entire hard drive or disk, which is part of the memory system, then Fisher inherently stores both high and low ILP instructions within that range on the disk. This is inherent looking at the instruction caches of Fisher in Figure 6 because all instructions cached in the processor inherently originate from a non-volatile disk or hard drive. Thus a memory range incorporating all addressable memory space with a processor inherently reads upon the claimed limitation because the disk inherently stores both high and low ILP instructions.

Additionally, when the memory range is a smaller range that encompasses the entire memory space of a processor, high and low ILP instruction[s] are inherently in the memory range ...

Finally, the memory range in Fisher can be as small as four instructions and still read on the claimed limitation, where the four instructions include a transition between switching from high to low ILP instructions, or vice versa. Thus, this memory range would include a couple [of] instructions from both the high and low ILP instructions. Therefore, the high ILP

instructions are stored within a memory range of the low ILP instructions. In fact, Jensen disclosed a great illustration that is obvious ...as to how instruction can be ordered and where a transition would occur. Jensen shows in figure 4 element 410 that instructions in program order transition into different ISA's at different physical addresses of a memory range." (see Examiner's Reply, page 14-15).

In reply, Appellant submits that claim 1 teaches the element:

"... an instruction memory system arranged to output an instruction word addressed by the instruction address, including at least one type of memory suitable for achieving a desired instruction cycle time wherein longer instruction words are contained within ranges of progressively shorter instruction words associated with a corresponding memory type..." (emphasis added).

Hence, claim 1 explicitly recites an order of the instructions within the memory wherein longer instructions are contained within ranges of progressively shorter instructions. Neither Fisher nor Jensen provides any teaching regarding this specific ordering of the instructions based on word length. Independent claim 15 recites similar features.

The Examiner has provided examples of the longer and shorter instructions that may be presented in different cache memories, and refers to the memory inherently being capable of containing longer and shorter instructions. However, nowhere does either Fisher or Jensen teach the ordered configuration recited in the claims.

However, the Examiner has not shown any specific teaching in Fisher of longer instruction words being stored in the memory within memory ranges of progressively shorter instruction words.

In addition, the Examiner argues that Appellant has failed to show to define what Fisher's intended purpose is that would preclude the inclusion of the teaching of Jensen into that of Fisher (see page 17, lines 7-12).

However, Appellant would note that the Examiner has argued "that the intended purpose of Fisher is to segregate high and low ILP instructions in different caches and enable a mode to select which cache to fetch instructions from" (see page 17, line 9-11).

Thus, in view of the Examiner's characterization of the teachings of Fisher as segregating the high and low instructions into different cache memories, Fisher cannot satisfy the recited claim element "wherein longer instruction words are contained within ranges of progressively shorter instruction words" (emphasis added).

In addition, even if it could be said that the shorter instructions in different caches have memory ranges that encompass the cache memory of the lower instructions, neither Fisher nor Jensen provide any teaching to order the different caches so that the longer instructions are contained with ranges of progressively shorter instructions.

Accordingly, neither Fisher nor Jensen provides any teaching regarding ordering the instructions in a manner as recited in the claims. Hence, the combination of Fisher and Jensen cannot render obvious the subject matter

recited in independent claims 1 and 15, as the combination of the cited references fails to disclose a material element recited in the claims.

For at least this reason Appellant submits that the reason for the rejection of the claims is not sustainable and requests this Honorable Board reverse and withdraw the rejection of the claims.

II. Rejection of claims 6 and 14 under 35 USC 103 over Fisher in view of Jensen and further in view of Lilja

Claims 6 and 14 stand rejected under 35 USC §103(a) as being unpatentable over Fisher, Jensen and Lilja.

Appellant re-asserts, as if in full, herein, the argument presented in Appellant's Appeal Brief.

In addition, independent claim 14 includes features similar to those recited in claims 1 and 15, which has been shown not to be disclosed by Fisher, herein and, thus Appellant re-asserts the argument presented in reply to the Examiner's Answer with regard to claims 1 and 15 in reply to the Examiner's Answer with regard to independent claim 14.

III. Rejection of claim 8 and 9 under 35 USC §103(a) as being unpatentable over Fisher, Jensen and Maiyuran.

Claims 8 and 9 stand rejected under 35 USC §103(a) as being unpatentable over Fisher, Jensen and Maiyuran.

Appellant re-asserts, as if in full, herein, the argument presented in Appellant's Appeal Brief.

IV. Rejection of claims 10 and 12 under 35 USC §103(a) as being unpatentable over Fisher in view Jensen and further in view of Sanches

Claims 10 and 12 stand rejected under 35 USC §103(a) as being unpatentable over Fisher, Jensen and Sanches.

Appellant re-asserts, as if in full, herein, the argument presented in Appellant's Appeal Brief.

V. Rejection of claim 11 under 35 USC §103(a) as being unpatentable over Fisher in view Jensen and in view of Sanches and further in view of Maiyuran

Claim 11 stands rejected under 35 USC §103(a) as being unpatentable over Fisher, Jensen and Sanches.

Appellant re-asserts, as if in full, herein, the argument presented in Appellant's Appeal Brief.

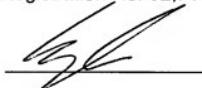
In view of the above, Appellant submits that the independent claims and the claims dependent therefrom are patently distinguishable and allowable over the teaching of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Respectfully submitted,

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Date: January 5, 2009

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IX. CLAIMS APPENDIX

The claims which are the subject of this Appeal are presented in Appellant's Appeal Brief.

X. EVIDENCE APPENDIX

Appellant agrees with the Examiner's statement in the Examiner's Answer.

XI. RELATED PROCEEDING APPENDIX

No related proceedings are pending and, hence, no information regarding same is available.